Electrical, Digital and Industrial Circuits
F3-6023

CAMEROON GENERAL CERTIFICATE OF EDUCATION BOARD

Probatoire Technique Examination

JUNE 2016 **Date: Thursday 26-05-2016**

Series/ Specialties	**Electrical Technology (F3)**
Subject Title	**Electrical, Digital and Industrial Circuits**
Subject Code No.	**F3-6023**
Type of Exam	**WRITTEN**
Weighting (Coef.)	**SEE INSIDE**

Duration: 8:00 - 9:00

General Instructions

You are reminded of the necessity for good English and orderly presentation of your material. Where calculations are involved show your working, giving your answer at each stage.

Content: QUESTIONS

Specific Instructions

Turn over

REPUBLIQUE DU CAMEROUN
Paix - Travail – Patrie

MINESEC/OBC

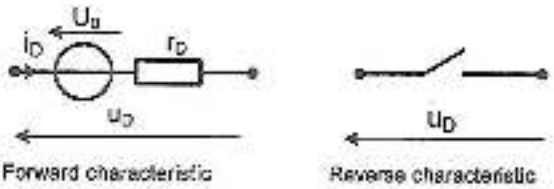
PROBATOIRE F
Session 201_
Speciality: F3
Duration : 04H
Coef : 04
Written paper

ELECTRICAL, DIGITAL AND INDUSTRIAL CIRCUITS

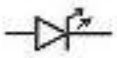
Authorized documents:. none
Number of pages : 04
Number of parts : 03
Paper marked over: 40

I TECHNOLOGY (8 marks)

1. Represent the simplified characteristic of the junction diode corresponding to the following model : (1mk)



2. Name the following element: (0.5mk)



Cite 03 applications of this element (1.5mk)

3. Give two advantages and two inconveniences of bipolar transistors with respect to field effect transistors. (1mk)
4. Define the following terms: propagation time, noise immunity, and operational amplifier offset voltage. (1.5mk)
5. Cite two multiplexers applications. (0.5mk)
6. Cite types of ROM memories and two types of RAM memories. (1mk)
7. Define a Functional Flow Chart and cite two conditions for crossing over a transition in it. (1mk)

II ANALOG CIRCUITS (17 marks)

2.1 Direct current *(6 marks)*

Consider the circuit of figure 1 below, with: E = 12V; R_1 = 6KΩ; R_2 = 3KΩ; R_C = 1KΩ.

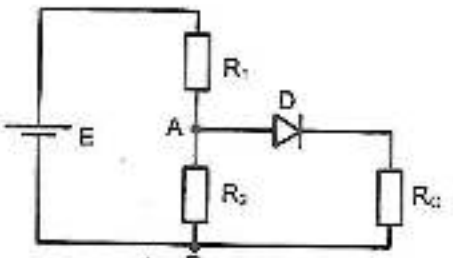


Figure 1

2.1.1 Calculate the equivalent Thevenin elements of the circuit, between the A and B terminals (the diode D and the resistance R_C being disconnected). (3mks)

2.1.2 Calculate the current flowing through the diode for the following differents models :

a) Ideal diode. (1mk)

b) Diode with a threshold $U_0 = 0.75V$. (1mk)

c) Diode with a threshold $U_0 = 0.75V$ and a dynamic resistance $r_d = 50\Omega$. (1mk)

2.2 *Bipolar transistor in static operation mode* *(6.5 marks)*

Consider the circuit assembly of figure 2 below:

$E = 20V$; $\beta 1 = 100$; $\beta_2 = 20$; $V_Z = 12V$; $V_{BE1} = V_{BE2} = V_{BE} = 0.7V$

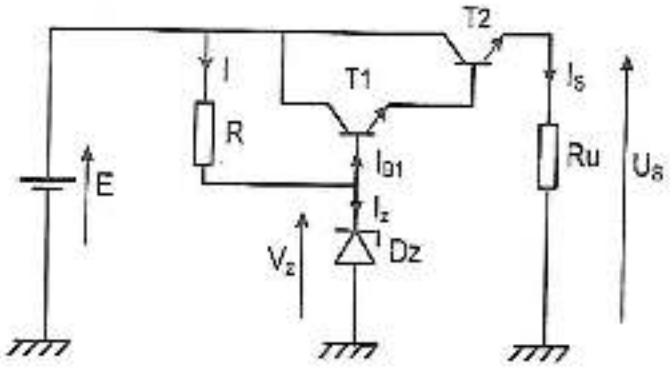


Figure 2

2.2.1 Calculate the output voltage U_s across the R_u terminals. (1mk)

2.2.2 The output current flowing through the load resistance Ru is $I_S = 5A$.

a) Calculate tho transistor T2 base curent I_{B2}. (1mk)

b) Then deduce the transistor T1 base current I_{B1} (1mk)

2.2.3 The zener diode D_z nominal current is $I_Z = 20mA$. Calculate the current I flowing through R. (1mk)

2.2.4 Calculate the value of the resistance R. (0.5mk)

2.2.5 Calculate the V_{CE1} voltage, knowing that $V_{CE1} = V_{C1}-V_{E1}$. Deduce the power P_1 Dissipated by the transistor T1. (2mks)

2.3 Operational amplifier (4.5 marks)

Consider the circuit assembly of the following figure 4 where v_e is a sinusoidal voltage with amplitude of 0.5V and v_s a voltage of amplitude of 6V. Operational amplifiers are supposed perfect.

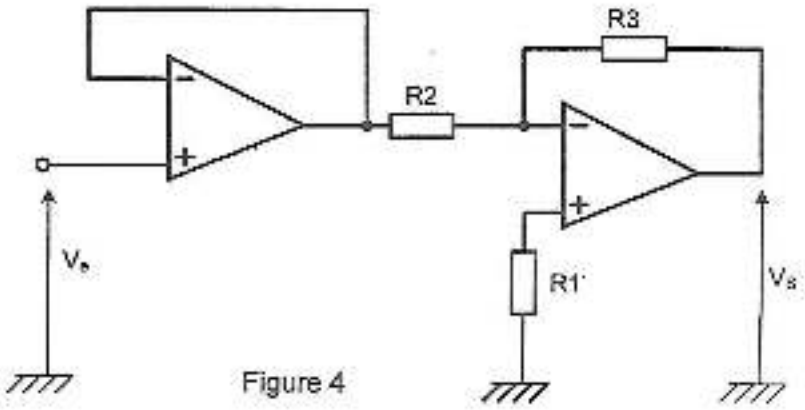


Figure 4

2.3.1 Calculate the voltage amplification Av of this device. (1.5mk)

2.3.2 Write expression of V_S as a function of V_e, R_2 and R_3. Deduce the value of R3 for R2 = 2KΩ. (2mks)

2.3.3 The resistance R1 helps compensating the differences between the operational amplifier input currents. For this assembly, it is proven that R1 = R3 // R2.
Calculate R1. (1mk)

III DIGITAL CIRCUITS *(15 marks)*

3.1 combinational Logic (6 marks)

Four directors (A ; B ; C ; D) of a company can have access in a coffer. They each possess a different key (respectively a, b, c, d). The director A can only open the coffer in the presence of director B or C. The directors B, C and D can only open the coffer in the presence of at least two other directors. It is desired to build a logic circuit whose output S enables to open coffer.

3.1.1 Draw the truth table corresponding to the functioning of the circuit. (2mks)

3.1.2 Give the equation of the output S simplified with the aid of Karnaugh map. (1mk)

3.1.3 Represent S using only two-input and three-input NAND gates. (3mks)

3.2 *Sequentiel Logic* *(9 marks)*

The figure 4 below represents the circuit of an asynchronous counter realized using JK latches.

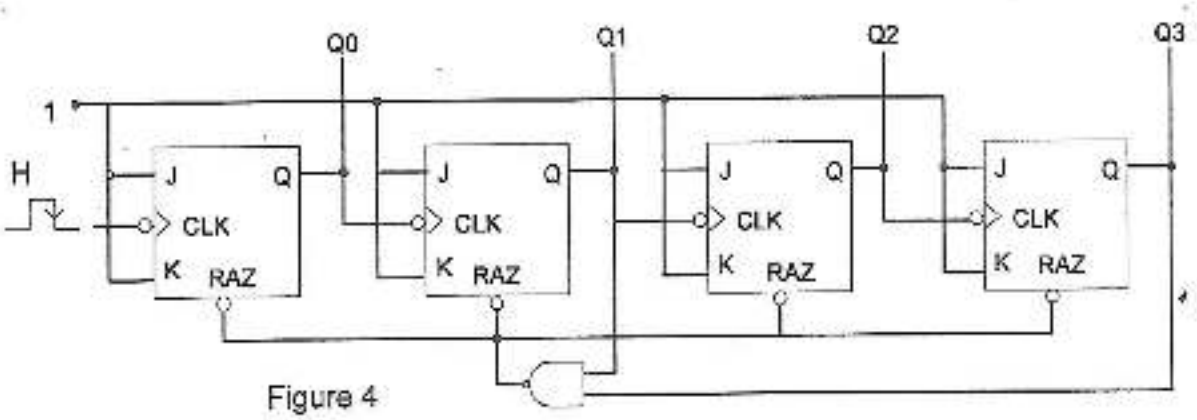


Figure 4

3.2.1 On which edge do the latches commutate? (1mk)

3.2.2 At what logic level are the RAZ inputs actives? (1mk)

3.2.3 Plot the time diagrams of Q0, Q1, Q2 and Q3 in function of the clock H signal. (at the initial state, Q0 = Q1 = Q2 = Q3 = "0") (6mks)

3.2.4 Find the modulo of this counter. (1mk)